Product Specification

2km 400G QSFP-DD FR4 Optical Transceiver Module

ECX-QSFP-DD-FR4-GN-03

PRODUCT FEATURES

- QSFP-DD MSA compliant
- Compliant to 100G Lambda MSA
- Compliant to 802.3cu
- 400G FR4 Specification compliant
- Non-hermetic package design
- 4 CWDM lanes MUX/DEMUX design
- 8x53.125Gb/s PAM4 electrical interface (400GAUI-8)
- Maximum power consumption 12W
- LC duplex connector
- Supports 425Gb/s aggregate bit rate
- Up to 2km transmission on single mode fiber with FEC
- Single 3.3V power supply
- RoHS-6 compliant

APPLICATIONS

- Data Center Interconnect

DESCRIPTION

It is a transceiver module designed for 2km optical communication applications, and it is compliant to 100G Lambda MSA standard. This module can convert 8-channel

53.125Gb/s electrical data to 4-channel 106.25Gb/s optical signals, and multiplex them into a single channel for 425Gb/s optical transmission. Similarly, it optically de-multiplexes a 425Gb/s input into 4-channel signals, and converts them to 8-channel output electrical data on the receiver side. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

Transceiver Block Diagram

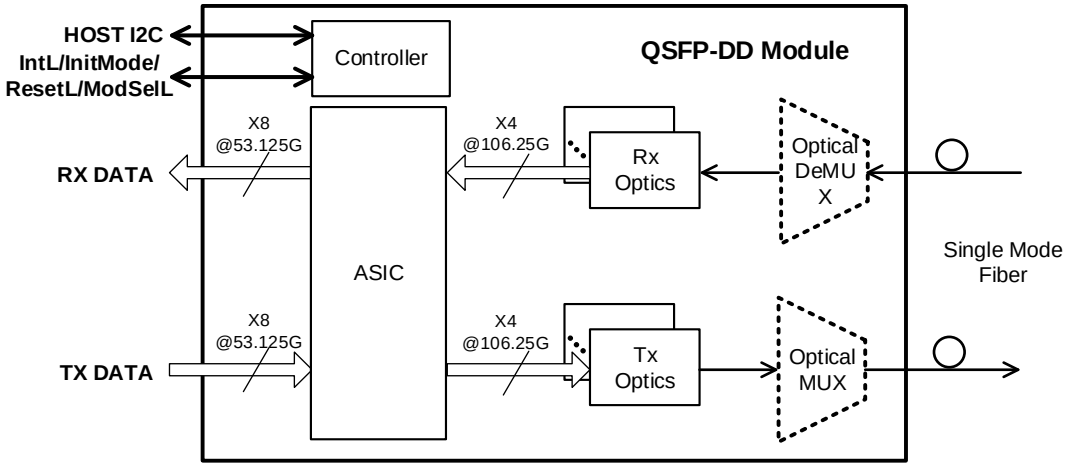

Figure 1. Transceiver Block Diagram

Proposed Application Schematics

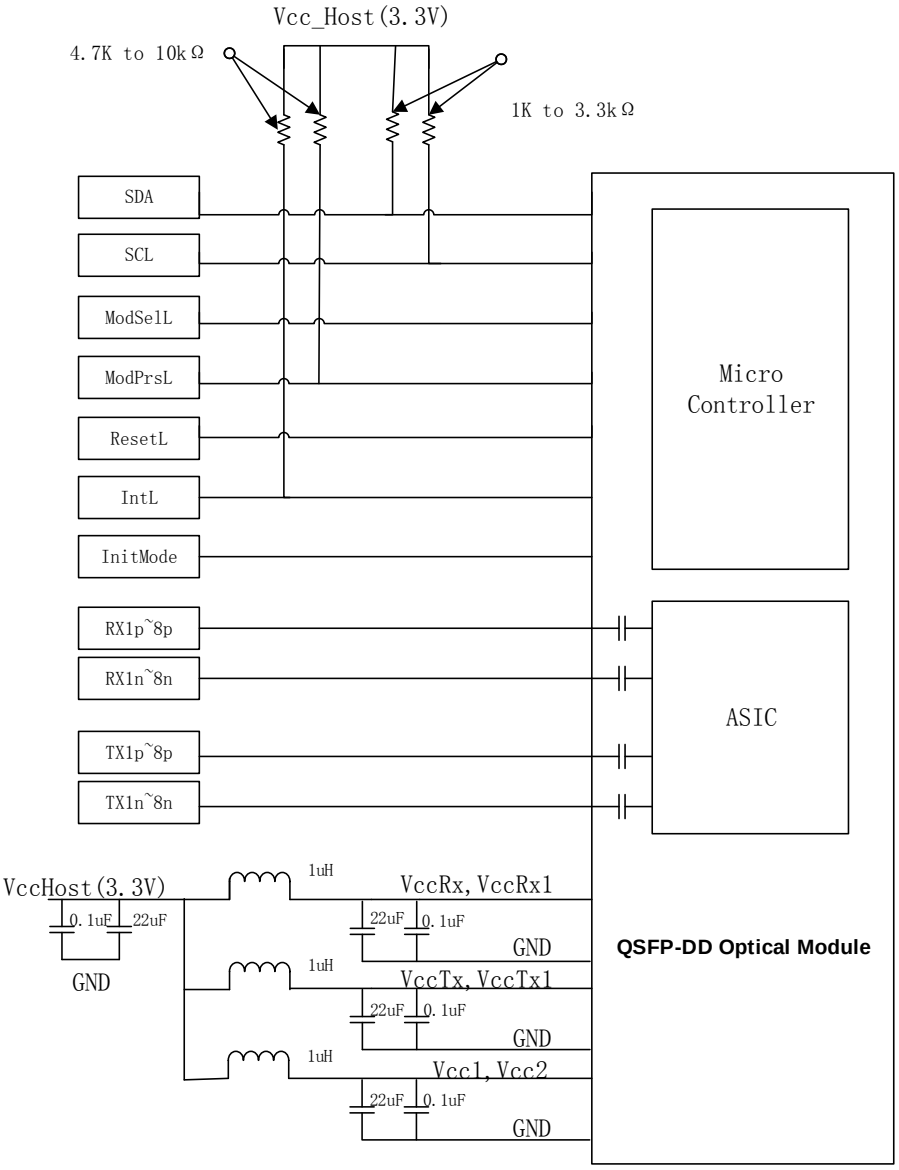

Figure 2. Proposed Application Schematics

Pin Descriptions

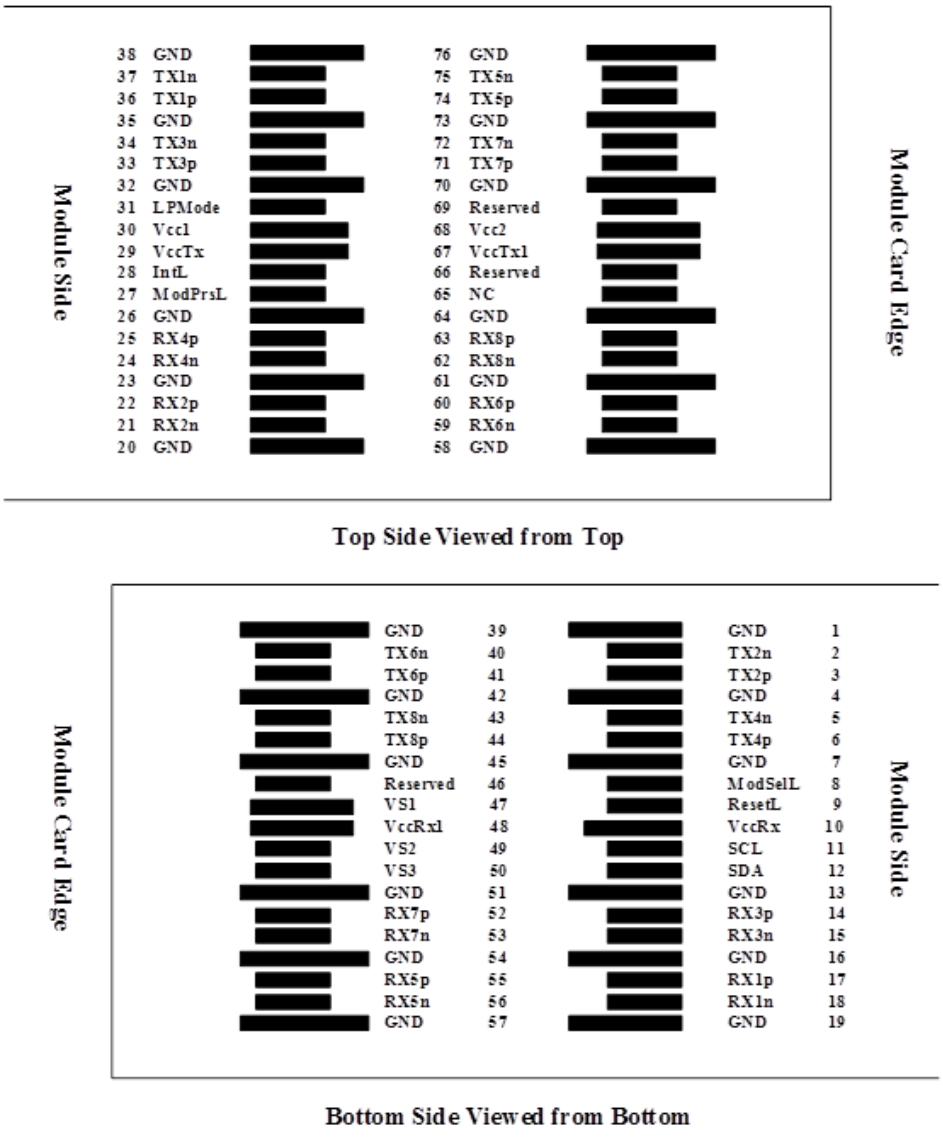

Figure 3. QSFP-DD MSA compliant Connector

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	

7		GND	Ground	1B	1
8	LVTTL-I	Mod-SelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		Vcc Rx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Non-Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-I	Mod-PrsL	Module Present	3B	
28	LVTTL-I	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	Init-Mode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	

41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	+3.3V Power supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Non-Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Non-Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For Future Use	3A	3
67		VccTx1	+3.3V Power supply	2A	2
68		Vcc2	+3.3V Power supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	

76		GND	Ground	1A	1
Note 1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.					
Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 6. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.					
Note 3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.					
Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A,2A,3A,1B,2B,3B. (see Figure 3 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B, followed by 3A,3B.					

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Maximum Supply Voltage	Vcc	-0.5	3.3	3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity	RH	0		85	%	

Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Case Temperature	T	0		70	℃	
Data Rate Accuracy		-100		100	ppm	
Link Distance		0.5		2000	m	1

Random failure rate				500	fits	2
Wearout lifetime		5			Year	3

Note:

1. G.652 Single-mode optical fiber
2. 60% CL, 50℃ case temperature
3. 70℃ case temperature.

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power dissipation	P			12	W	
Supply Current	Icc			3.63	A	
Transmitter						
Data Rate, each lane		26.5625±100ppm			GBd	
Differential input Voltage pk-pk	Vpp	900			mV	1
Common Mode Voltage	Vcm	-350	700	2850	mV	2
Differential Termination Resistance Mismatch				10	%	
Single-ended Voltage Tolerance Range (Min)		-0.4		3.3	V	
Differential Input Return Loss		IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss		IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test		IEEE 802.3cu				3
Receiver						
Data Rate, each lane		26.5625±100ppm			GBd	
Differential Termination Resistance Mismatch				10	%	
Differential output Voltage pk-pk	Vpp			900	mV	
Common Mode Voltage	Vcm	-350		2850	mV	2
Common Mode Noise,	Vrms			17.5	mV	

RMS						
Transition time (min)		9.5			ps	20%to80%
Near-end Eye height, differential (min)		70			mV	
Near-end ESMW (Eye symmetry mask width)		0.265			UI	
Far-end ESMW (Eye symmetry mask width)		0.2			UI	
Far-end Eye height, differential (min)		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss		IEEE 802.3-2015 Equation (83E-2)				
Common to differential mode conversion return loss		IEEE 802.3-2015 Equation (83E-3)				
Note: 1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle. 2. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage. 3. BER specified in IEEE 802.3bs 120E.1.1.						

Optical Characteristics

Parameters	Unit	min	type	max
Transmitter				
Data Rate, each Lane	GBd	53.125±100ppm		
Modulation Format		PAM4		
Line wavelengths	nm	1264.5	1271	1277.5
		1284.5	1291	1297.5
		1304.5	1311	1317.5
		1324.5	1331	1337.5
Total Average Launch Power	dBm			9.5
Average Launch Power, each	dBm	-3.3		3.5

lane				
Optical Modulation Amplitude (OMA), each lane	dBm	-0.3		3.7
Extinction Ratio (ER)	dB	3.5		
Side-Mode Suppression Ratio (SMSR)	dB	30		
Launch power in OMA minus TDECQ, each lane, for ER≥ 4.5dB	dB	-1.7		
Launch power in OMA minus TDECQ, each lane, for ER <4.5dB	dB	-1.6		
Transmitter and Dispersion Eye Clouser for PAM4, each Lane (TDECQ)	dB			3.4
Difference in Launch Power between any Two Lanes (OMAouter)	dB			4
RIN17.1OMA	dB/Hz			-136
Optical Return Loss Tolerance	dB			17.1
Transmitter Reflectance	dB			-26
Average Launch Power of OFF Transmitter, each Lane	dBm			-20
Receiver				
Data Rate, each Lane	GBd	53.125±100ppm		
Modulation Format		PAM4		
Damage Threshold, each lane	dBm	4.5		
Line wavelengths	nm	1264.5	1271	1277.5
		1284.5	1291	1297.5
		1304.5	1311	1317.5
		1324.5	1331	1337.5
Average receiver power, each lane	dBm	-7.3		3.5
Receiver power, each lane (OMA)	dBm			3.7
Difference in Receiver Power	dB			4.1

between any Two Lanes (OMA)				
Stressed receiver Sensitivity (OMAouter) , each lane(max)	dBm	See Note		
LOS Assert	dBm	-15		
LOS Deassert	dBm			-8.6
LOS Hysteresis	dB	0.5		
Receiver reflectance	dB			-26
Conditions of Stressed Receiver Sensitivity				
Stressed eye closure for PAM4 (SECQ), lane under test	dB	0.9		3.4
OMAouter of each aggressor lane	dBm		1.5	
Note: Measured with conformance test signal for BER = 2.4x10-4. A compliant receiver shall have stressed receiver sensitivity (OMA outer), each lane values below the mask of Figure 4, for SECQ values between 0.9 and 3.4 dB.				

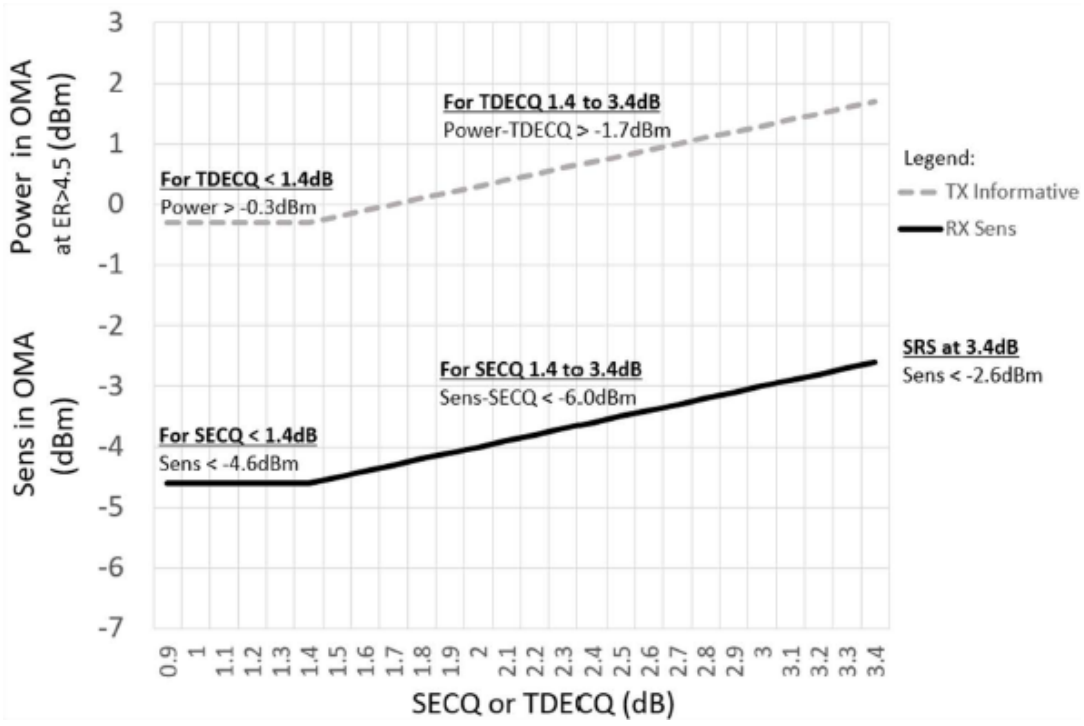

Figure 4. Stressed receiver sensitivity mask for 400G-FR4

EEPROM Definitions

Lower Memory Map

data address	Name	Description	Value (hex)	Read/Write
0	ID & version ID	Identifier	18	RO
1		Revision Compliance	40	RO
2	Status region	flate_men/CLEI/TWI max speed	00	RO
3		Module state/interrupt	*	RO
4	Bank lane Flag Summary	Bank 0 lane1~8 flag summary change 0b：No change 1b：change	*	RO
5		Bank 1 lane1~8 flag summary change	*	RO
6		Bank 2 lane1~8 flag summary change	*	RO
7		Bank 3 lane1~8 flag summary change	*	RO
8	Module Flags	firmware fault & L-Module state change flage	*	RO
9		3.3V&temperture low/high alarm/warning flag	*	RO
10		L-Aux1 &L-Aux2 low/high alarm/warning flag	*	RO
11		L-Vendor define & L-Aux3 low/high alarm/warning flag	*	RO
12		reserved	00	RO
13		custom	00	RO
14	Module Monitors	temperature1 MSB（1/256℃）	*	RO
15		temperature1 LSB（1/256℃）	*	RO
16		Supply 3.3 MSB（0.1mV）	*	RO
17		Supply 3.3 LSB（0.1mV）	*	RO
18		AUX 1 MSB-ITEC（0.1mA）	*	RO
19		AUX 1 LSB-ITEC（0.1mA）	*	RO
20		AUX 2 MSB-LsrTmp（1/256℃）	*	RO
21		AUX 2 LSB-LsrTmp（1/256℃）	*	RO

22		AUX 3 MSB	*	RO
23		AUX 3 LSB	*	RO
24		Custom MSB	*	RO
25		Custom LSB	*	RO
26	Module Global Controls	Squelch control / ForceLowPwr/soft reset 08h:Soft reset 00h:ForceHighPwr 10h: ForceLowPwr	40	RW
27		reserved	00	RW
28				RW
29		Custom	00	RW
30				RW
31	Module masks	Mask bit for Module State Changed Flag	00	RW
32		Mask bit for temp&supply 3.3V low/high alarm/warning flag	00	RW
33		Mask bit for AUX1&AUX2 low/high alarm/warning flag	00	RW
34		Mask bit for AUX3&Vendor define low/high alarm/warning flag	00	RW
35		reserved	00	RW
36		Custom	00	RW
37	Bank 0 CDB state	CDB state： 1.CMD Captured：0x81 2.CMD Checking：0x82 3.CMD Execution：0x83 4.CMD Failed：0x41-0x46 5.CMD Abort：0x03 6.CMD Succ：0x01	*	RO
38	Bank 1 CDB state		*	RO
39	Module FW Version	Active Module FW major Version	11	RO
40		Active Module FW minor Version	07	RO
41	Reserve Area		00	RO
42				
43				
44				
45				
46				
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48				
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51				
52				
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59				
60				
61				
62				
63				
64	Custom		00	RO
65				
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72				
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74				
75				
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77				
78				
79				
80				
81				
82				
83	Inactive FW Version	Inactive Module FW major Version	00	RO
84		Inactive Module FW minor Version	00	RO
85	Module Type Advertising code	Module Type Code	02	RO
86	Module Host-media interface Advertising options	Host Electrical Interface Code	11	RO
87		Module Media Interface Code	1D	RO
88		Host/Media LANE Count	84	RO
89		Host lane Assignment Options	01	RO
90		Host Electrical Interface Code	FF	RO
91		Module Media Interface Code	00	RO

92		Host/Media LANE Count	00	RO
93		Host lane Assignment Options	00	RO
94		Host Electrical Interface Code	00	RO
95		Module Media Interface Code	00	RO
96		Host/Media LANE Count	00	RO
97		Host lane Assignment Options	00	RO
98		Host Electrical Interface Code	00	RO
99		Module Media Interface Code	00	RO
100		Host/Media LANE Count	00	RO
101		Host lane Assignment Options	00	RO
102		Host Electrical Interface Code	00	RO
103		Module Media Interface Code	00	RO
104		Host/Media LANE Count	00	RO
105		Host lane Assignment Options	00	RO
106		Host Electrical Interface Code	00	RO
107		Module Media Interface Code	00	RO
108		Host/Media LANE Count	00	RO
109		Host lane Assignment Options	00	RO
110		Host Electrical Interface Code	00	RO
111		Module Media Interface Code	00	RO
112		Host/Media LANE Count	00	RO
113		Host lane Assignment Options	00	RO
114		Host Electrical Interface Code	00	RO
115		Module Media Interface Code	00	RO
116		Host/Media LANE Count	00	RO
117		Host lane Assignment Options	00	RO
118	password Change Area		00	WO
119			00	
120			00	
121			00	
122	Password Area	Host Password:00001011	00	WO
123			00	
124			00	
125			00	
126	Bank Select Byte		00	RW
127	Page Select Byte		00	RW

Upper Memory Map Page 00h

data ad-dress	Name	Description	Value (hex)	Read/Write

128	Identifier	ID	18	RO
129	Vendor name	Vendor name	“HUAWEI”	RO
130				
131				
132				
133				
134				
135				
136				
137				
138				
139				
140				
141				
142				
143				
144				
145	Vender OUI	Vendor Organizationally Unique ID	*	RO
146				
147				
148	Vender PN	Vender Part Number	*	RO
149				
150				
151				
152				
153				
154				
155				
156				
157				
158				
159				
160				
161				
162				
163				
164	Vender rev	Vender Revision Number	“A0”	RO
165				
166	Vender SN	Vender Serial Number	*	RO
167				
168				
169				

170				
171				
172				
173				
174				
175				
176				
177				
178				
179				
180				
181				
182	Data Code	Data Code year	*	RO
183				
184		Data Code month	*	RO
185				
186		Data Code day of month	*	RO
187				
188		Lot code	*	RO
189				
190	CLEI Code	Common Language Equipment ID	*	RO
191				
192				
193				
194				
195				
196				
197				
198				
199				
200	Module power characteristics	Module Power Class	A0	RO
201		Module MAX Power	30	RO
202	cable assembly length	cable assembly length	00	RO
203	Media Connector Type	Connector Type	07	RO
204	Copper Cable Attenuation	5G attenuation	00	RO
205		7G attenuation	00	RO
206		12.9G attenuation	00	RO
207		25.8G attenuation	00	RO
208		Reserved	00	RO
209				

210	Cable Assembly Lane Information	near end implementation lane1~8	00	RO
211		Far end Configuration	00	RO
212	Media Interface Technology	wanlength&device	06	RO
213	Reserved		00	RO
214				
215				
216				
217				
218				
219				
220				
221	Custom		00	RO
222	Checksum	Checksum for 128~221	*	RO
223	Custom Info NV		00	RO
224				
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230				
231				
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Upper Memory Map Page 01h

data address	Name	Description	Value (hex)	Read/Write
128	Module FW&HW REV	Module firmware major revision	*	RO
129		Module firmware minor revision	*	RO
130		Module hardware major revision	01	RO
131		Module hardware minor revision	00	RO
132	Supported Link Length	Base Length (SMF)	14	RO
133		Length (OM5)	00	RO
134		Length (OM4)	00	RO
135		Length (OM3)	00	RO
136		Length (OM2)	00	RO
137		Reserved	00	RO
138	Nominal Wavelength	wavelength MSB	66	RO
139		wavelength LSB	58	RO
140	Wavelength Tolerance	Wavelength Tolerance MSB	05	RO
141		Wavelength Tolerance LSB	14	RO
142	Implemengted management interface futures advertising	Diagnostic/page03/banks implemented	24	RO
143		ModSel wait time	f0	RO
144		DataPathDeinit/DataPathInit MaxDuration	68	RO
145	Module Characteristics advertising	Synchronous/Aux	81	RO
146		Maximum module temperature	46	RO
147		Minimum module temperature	00	RO
148		Propagation Delay MSB	00	RO
149		Propagation Delay LSB	00	RO
150		Minimum operating voltage	9d	RO
151		Rx Type	1e	RO
152		per lane CDR Power saved	00	RO
153		Rx Output Amplitude code/Max Txeq	80	RO
154		Max Rx Out Eq Post/Pre-cursor	77	RO

155	Implemented Controls advertising	Tx Squelch/Disable/Polarity	1F	RO
156		Rx Squelch/Disable/Polarity	07	RO
157	Imlemented Flags advertising	Tx Fault/Los/LoL Flag	07	RO
158		Rx Los/LoL Flag	06	RO
159	Implemented Monitors advertising	Monitor enable	0f	RO
160		Tx Bias current multiplier /Rx Power/Tx Power/Tx Bias enable	0f	RO
161	Implemented Signal Integrity Controls advertising	TX EQ/CDR Control	09	RO
162		RX EQ/CDR Control	1d	RO
163	CDB Advertisement	CDB implemented	40	RO
164		CDB Max TWI Bytes per write transaction	0f	RO
165		CDB command processing option	9f	RO
166		CDB tNACK time indicator	80	RO
167	Additional state machine durations advertising	ModulePwrDn_MaxDuration\ModulePwrUp_MaxDuration	57	RO
168		DataPathTxTurnOff_MaxDuration\DataPathTxTurnOn_MaxDuration	55	RO
169	RSV		00	RO
170				
171				
172				
173				
174				
175				
176	Module Media Lane advertising	Media Lane Assignment Options, ApSel 0001b	00	RO
177		Media Lane Assignment Options, ApSel 0010b	00	RO
178		Media Lane Assignment Options, ApSel 0011b	00	RO
179		Media Lane Assignment Options, ApSel 0100b	00	RO
180		Media Lane Assignment Options, ApSel 0101b	00	RO
181		Media Lane Assignment Options, ApSel 0110b	00	RO
182		Media Lane Assignment Options, ApSel 0111b	00	RO

183		Media Lane Assignment Options, ApSel 1000b	00	RO
184		Media Lane Assignment Options, ApSel 1001b	00	RO
185		Media Lane Assignment Options, ApSel 1010b	00	RO
186		Media Lane Assignment Options, ApSel 1011b	00	RO
187		Media Lane Assignment Options, ApSel 1100b	00	RO
188		Media Lane Assignment Options, ApSel 1101b	00	RO
189		Media Lane Assignment Options, ApSel 1110b	00	RO
190		Media Lane Assignment Options, ApSel 1111b	00	RO
191	Custom		00	RO
192				
193				
194				
195				
196				
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199				
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218				
219				
220				
221				
222				
223	Extend Module Host-Media Interface Advertising options	HOST Electrical Interface Code	00	RO
224		Module Media Interface Code	00	RO
225		HOST /Media Lane Count	00	RO
226		HOST Lane Assignment Options	00	RO
227		HOST Electrical Interface Code	00	RO
228		Module Media Interface Code	00	RO
229		HOST /Media Lane Count	00	RO
230		HOST Lane Assignment Options	00	RO
231		HOST Electrical Interface Code	00	RO
232		Module Media Interface Code	00	RO
233		HOST /Media Lane Count	00	RO
234		HOST Lane Assignment Options	00	RO
235		HOST Electrical Interface Code	00	RO
236		Module Media Interface Code	00	RO
237		HOST /Media Lane Count	00	RO
238		HOST Lane Assignment Options	00	RO
239		HOST Electrical Interface Code	00	RO
240		Module Media Interface Code	00	RO
241		HOST /Media Lane Count	00	RO
242		HOST Lane Assignment Options	00	RO
243		HOST Electrical Interface Code	00	RO
244		Module Media Interface Code	00	RO
245		HOST /Media Lane Count	00	RO
246		HOST Lane Assignment Options	00	RO
247		HOST Electrical Interface Code	00	RO
248		Module Media Interface Code	00	RO
249		HOST /Media Lane Count	00	RO
250		HOST Lane Assignment Options	00	RO
251	Rserved		00	RO
252				
253				
254				
255	Checksum	130~254	*	RO

Upper Memory Map Page 02h

data address	Name	Description	Value (hex)	Read/Write
128	Module-Level monitor thresholds	Temperature monitor high alarm threshold MSB	50	RO
129		Temperature monitor high alarm threshold LSB	00	RO
130		Temperature monitor low alarm threshold MSB	f6	RO
131		Temperature monitor low alarm threshold LSB	00	RO
132		Temperature monitor high warning threshold MSB	46	RO
133		Temperature monitor high warning threshold LSB	00	RO
134		Temperature monitor low warning threshold MSB	00	RO
135		Temperature monitor low warning threshold LSB	00	RO
136		Supply 3.3-volt monitor high alarm threshold MSB	8d	RO
137		Supply 3.3-volt monitor high alarm threshold LSB	cc	RO
138		Supply 3.3-volt monitor low alarm threshold MSB	74	RO
139		Supply 3.3-volt monitor low alarm threshold LSB	04	RO
140		Supply 3.3-volt monitor high warning threshold MSB	87	RO
141		Supply 3.3-volt monitor high warning threshold LSB	5a	RO
142		Supply 3.3-volt monitor low warning threshold MSB	7a	RO
143		Supply 3.3-volt monitor low warning threshold LSB	76	RO
144		Aux 1 monitor high alarm threshold MSB	7F	RO
145		Aux 1 monitor high alarm threshold LSB	FF	RO
146		Aux 1 monitor low alarm threshold MSB	80	RO
147		Aux 1 monitor low alarm threshold LSB	01	RO
148		Aux 1 monitor high warning threshold MSB	7F	RO

149		Aux 1 monitor high warning threshold LSB	FF	RO
150		Aux 1 monitor low warning threshold MSB	80	RO
151		Aux 1 monitor low warning threshold LSB	01	RO
152		Aux 2 monitor high alarm threshold MSB	7F	RO
153		Aux 2 monitor high alarm threshold LSB	FF	RO
154		Aux 2 monitor low alarm threshold MSB	80	RO
155		Aux 2 monitor low alarm threshold LSB	00	RO
156		Aux 2 monitor high warning threshold MSB	7F	RO
157		Aux 2 monitor high warning threshold LSB	FF	RO
158		Aux 2 monitor low warning threshold MSB	80	RO
159		Aux 2 monitor low warning threshold LSB	00	RO
160		Aux 3 monitor high alarm threshold MSB	00	RO
161		Aux 3 monitor high alarm threshold LSB	00	RO
162		Aux 3 monitor low alarm threshold MSB	00	RO
163		Aux 3 monitor low alarm threshold LSB	00	RO
164		Aux 3 monitor high warning threshold MSB	00	RO
165		Aux 3 monitor high warning threshold LSB	00	RO
166		Aux 3 monitor low warning threshold MSB	00	RO
167		Aux 3 monitor low warning threshold LSB	00	RO
168		Custom monitor high alarm threshold MSB	00	RO
169		Custom monitor high alarm threshold LSB	00	RO
170		Custom monitor low alarm threshold MSB	00	RO
171		Custom monitor low alarm threshold LSB	00	RO
172		Custom monitor high warning threshold MSB	00	RO
173		Custom monitor high warning threshold LSB	00	RO
174		Custom monitor low warning threshold MSB	00	RO
175		Custom monitor low warning threshold LSB	00	RO

176	Lane-specific monitor thresh-olds	Tx optical power monitor high alarm threshold MSB	C3	RO
177		Tx optical power high alarm threshold LSB	C7	RO
178		Tx optical power low alarm threshold MSB	09	RO
179		Tx optical power low alarm threshold LSB	28	RO
180		Tx optical power high warning threshold MSB	62	RO
181		Tx optical power high warning threshold LSB	1F	RO
182		Tx optical power low warning threshold MSB	11	RO
183		Tx optical power low warning threshold LSB	73	RO
184		Tx bias current monitor high alarm threshold MSB	8D	RO
185		Tx bias current high alarm threshold LSB	9A	RO
186		Tx bias current low alarm threshold MSB	00	RO
187		Tx bias current low alarm threshold LSB	FA	RO
188		Tx bias current high warning threshold MSB	88	RO
189		Tx bias current high warning threshold LSB	B8	RO
190		Tx bias current low warning threshold MSB	09	RO
191		Tx bias current low warning threshold LSB	C4	RO
192		Rx optical power monitor high alarm threshold MSB	C3	RO
193		Rx optical power high alarm threshold LSB	C7	RO
194		Rx optical power low alarm threshold MSB	03	RO
195		Rx optical power low alarm threshold LSB	67	RO
196		Rx optical power high warning threshold MSB	62	RO
197		Rx optical power high warning threshold LSB	1F	RO
198		Rx optical power low warning threshold MSB	06	RO

199		Rx optical power low warning threshold LSB	CA	RO
200	Reserved		00	RO
201				
202				
203				
204				
205				
206				
207				
208				
209				
210				
211				
212				
213				
214				
215				
216				
217				
218				
219				
220				
221				
222				
223				
224				
225				
226				
227				
228				
229				
230	Customizable space		00	RO
231				
232				
233				
234				
235				
236				
237				
238				
239				

240				
241				
242				
243				
244				
245				
246				
247				
248				
249				
250				
251				
252				
253				
254				
255	Checksum	Covers bytes 128-254	*	RO

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data address	Name	Description	Value (hex)	Read/Write
128	Data Path Power control	DataPathPwrUp lane1 ~ 8 0xFF：PwrDwn 0x00：PwrUp	00	RW
129	Lane-Specific Control	Tx1~8 Polarity Flip	00	RW
130		TX Disable for media lane 1~8	00	RW
131		TX Squelch for media lane 1~8	FF	RW
132		TX Force Squelch for media lane 1~8	00	RW
133		reserved	00	RO
134		TX Input Eq Adaptation Freeze for lane 1~8	00	RW
135		TX1~4 Input Eq Adaptation Store	00	WO
136		TX5~8 Input Eq Adaptation Store	00	WO
137		Rx1~8 Polarity Flip	00	RW
138		RX Output Disable for 1~8	00	RW
139		RX Squelch Disable for 1~8	00	RW
140		reserved	00	RO
141			00	
142			00	
143	Staged Control Set 0	Staged Set 0 Lane 1~8 Apply_DataPath-Init	00	WO
144		Staged Set 0 Lane 1~8 Apply_Immediate	00	WO
145		Staged Set 0 Lane 1 Application code/Data Path code/Explicit Control	10	RW
146		Staged Set 0 Lane 2 Application code/Data Path code/Explicit Control	10	
147		Staged Set 0 Lane 3 Application code/Data Path code/Explicit Control	10	
148		Staged Set 0 Lane 4 Application code/Data Path code/Explicit Control	10	
149		Staged Set 0 Lane 5 Application code/Data Path code/Explicit Control	10	
150		Staged Set 0 Lane 6 Application code/Data Path code/Explicit Control	10	
151		Staged Set 0 Lane 7 Application code/Data Path code/Explicit Control	10	

152		Staged Set 0 Lane 8 Application code/Data Path code/Explicit Control	10	
153		Staged Set 0 Tx1~8 Adaptive Input Eq Enable	ff	
154		Staged Set 0 Tx1~4 Adaptive Input Eq Recall	00	
155		Staged Set 0 Tx5~8 Adaptive Input Eq Recall	00	
156		Staged Set 0 Tx1~2 Input Eq control	00	
157		Staged Set 0 Tx3~4 Input Eq control	00	
158		Staged Set 0 Tx5~6 Input Eq control	00	
159		Staged Set 0 Tx7~8 Input Eq control	00	
160		Staged Set 0 Tx1~8 CDR control	FF	
161		Staged Set 0 Rx1~8 CDR control	FF	
162		Staged Set 0 Rx1~2 Output Eq control, pre-cursor	00	
163		Staged Set 0 Rx3~4 Output Eq control, pre-cursor	00	
164		Staged Set 0 Rx5~6 Output Eq control, pre-cursor	00	
165		Staged Set 0 Rx7~8 Output Eq control, pre-cursor	00	
166		Staged Set 0 Rx1~2 Output Eq control, post-cursor	00	
167		Staged Set 0 Rx3~4 Output Eq control, post-cursor	00	
168		Staged Set 0 Rx5~6 Output Eq control, post-cursor	00	
169		Staged Set 0 Rx7~8 Output Eq control, post-cursor	00	
170		Staged Set 0 Rx1~2 Output Amplitude control	33	
171		Staged Set 0 Rx3~4 Output Amplitude control	33	
172		Staged Set 0 Rx5~6 Output Amplitude control	33	
173		Staged Set 0 Rx7~8 Output Amplitude control	33	
174		reserved	00	RO
175			00	
176			00	
177			00	

178	Staged Control Set 1	Staged Set 1 Lane 1~8 Apply_DataPath-Init	00	WO
179		Staged Set 1 Lane 1~8 Apply_Immediate	00	WO
180		Staged Set 1 Lane 1 Application code/Data Path code/Explicit Control	10	RW
181		Staged Set 1 Lane 2 Application code/Data Path code/Explicit Control	10	
182		Staged Set 1 Lane 3 Application code/Data Path code/Explicit Control	10	
183		Staged Set 1 Lane 4 Application code/Data Path code/Explicit Control	10	
184		Staged Set 1 Lane 5 Application code/Data Path code/Explicit Control	10	
185		Staged Set 1 Lane 6 Application code/Data Path code/Explicit Control	10	
186		Staged Set 1 Lane 7 Application code/Data Path code/Explicit Control	10	
187		Staged Set 1 Lane 8 Application code/Data Path code/Explicit Control	10	
188		Staged Set 1 Tx1~8 Adaptive Input Eq Enable	FF	
189		Staged Set 1 Tx1~4 Adaptive Input Eq Recall	00	
190		Staged Set 1 Tx5~8 Adaptive Input Eq Recall	00	
191		Staged Set 1 Tx1~2 Input Eq control	00	
192		Staged Set 1 Tx3~4 Input Eq control	00	
193		Staged Set 1 Tx5~6 Input Eq control	00	
194		Staged Set 1 Tx7~8 Input Eq control	00	
195		Staged Set 1 Tx1~8 CDR control	Ff	
196		Staged Set 1 Rx1~8 CDR control	Ff	
197		Staged Set 1 Rx1~2 Output Eq control, pre-cursor	00	
198		Staged Set 1 Rx3~4 Output Eq control, pre-cursor	00	
199		Staged Set 1 Rx5~6 Output Eq control, pre-cursor	00	
200		Staged Set 1 Rx7~8 Output Eq control, pre-cursor	00	
201		Staged Set 1 Rx1~2 Output Eq control, post-cursor	00	

202		Staged Set 1 Rx3~4 Output Eq control, post-cursor	00	
203		Staged Set 1 Rx5~6 Output Eq control, post-cursor	00	
204		Staged Set 1 Rx7~8 Output Eq control, post-cursor	00	
205		Staged Set 1 Rx1~2 Output Amplitude control	33	
206		Staged Set 1 Rx3~4 Output Amplitude control	33	
207		Staged Set 1 Rx5~6 Output Amplitude control	33	
208		Staged Set 1 Rx7~8 Output Amplitude control	33	
209		reserved	00	RO
210				
211				
212				
213	Lane-Specific Flag Masks	M-Lane 1~8 Data Path State Changed flag mask	00	RW
214		M-Tx1~8 Fault flag mask	00	RW
215		M-Tx1~8 LOS flag mask	00	RW
216		M-Tx1~8 CDR LOL flag mask	00	RW
217		M-Tx1~8 Adaptive Eq Fault flag mask	00	RW
218		M-Tx1~8 Power High Alarm flag mask	00	RW
219		M-Tx1~8 Power Low Alarm flag mask	00	RW
220		M-Tx1~8 Power High Warning flag mask	00	RW
221		M-Tx1~8 Power Low Warning flag mask	00	RW
222		M-Tx1~8 Bias High Alarm flag mask	00	RW
223		M-Tx1~8 Bias Low Alarm flag mask	00	RW
224		M-Tx1~8 Bias High Warning flag mask	00	RW
225		M-Tx1~8 Bias Low Warning flag mask	00	RW
226		M-Rx1~8 LOS flag mask	00	RW
227		M-Rx1~8 CDR LOL flag mask	00	RW
228		M-Rx1~8 Power High Alarm flag mask	00	RW
229		M-Rx1~8 Power Low Alarm flag mask	00	RW
230		M-Rx1~8 Power High Warning flag mask	00	RW
231		M-Rx1~8 Power Low Warning flag mask	00	RW
232	Reserved		00	RO
233				
234				
235				

236				
237				
238				
239				
240	Custom		00	RO
241				
242				
243				
244				
245				
246				
247				
248				
249				
250				
251				
252				
253				
254				
255				

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data address	Name	Description	Value (hex)	Read/Write
128	Datapath State indicators	Data path state encoding for lane 1~2	*	RO
129		Data path state encoding for lane 3~4	*	RO
130		Data path state encoding for lane 5~6	*	RO
131		Data path state encoding for lane 7~8	*	RO
132	reserved		00	RO
133				
134	Lane-specific flags	Latched Data Path State Changed flag for lane 1~8	*	RO
135		Latched Tx Fault flag, media lane 1~8	*	RO
136		Latched Tx LOS flag, lane 1~8	*	RO
137		Latched Tx CDR LOL flag, lane 1~8	*	RO
138		Latched Tx Adaptive Input Eq. Fault Lane 1~8	*	RO
139		Tx output power High Alarm, media lane 1~8	*	RO

140		Tx output power Low alarm, media lane 1~8	*	RO
141		Tx output power High warning, media lane 1~8	*	RO
142		Tx output power High warning, media lane 1~8	*	RO
143		Tx Bias High Alarm, media lane 1~8	*	RO
144		Tx Bias Low alarm, media lane 1~8	*	RO
145		Tx Bias High warning, media lane 1~8	*	RO
146		Tx Bias Low warning, media lane 1~8	*	RO
147		Latched Rx LOS flag, media lane 1~8	*	RO
148		Latched Rx CDR LOL flag, media lane 1~8	*	RO
149		Rx input power High alarm, media lane 1~8	*	RO
150		Rx input power Low alarm, media lane 1~8	*	RO
151		Rx input power High warning, media lane 1~8	*	RO
152		Rx input power Low warning, media lane 1~8	*	RO
153	reserved		00	RO
154	Lane-specific monitors	Tx1 Power MSB	*	RO
155		Tx1 Power LSB	*	RO
156		Tx2 Power MSB	*	RO
157		Tx2 Power LSB	*	RO
158		Tx3 Power MSB	*	RO
159		Tx3 Power LSB	*	RO
160		Tx4 Power MSB	*	RO
161		Tx4 Power LSB	*	RO
162		Tx5 Power MSB	*	RO
163		Tx5 Power LSB	*	RO
164		Tx6 Power MSB	*	RO
165		Tx6 Power LSB	*	RO
166		Tx7 Power MSB	*	RO
167		Tx7 Power LSB	*	RO
168		Tx8 Power MSB	*	RO
169		Tx8 Power LSB	*	RO
170		Tx1 Bias MSB	*	RO
171		Tx1 Bias LSB	*	RO
172		Tx2 Bias MSB	*	RO
173		Tx2 Bias LSB	*	RO

174		Tx3 Bias MSB	*	RO
175		Tx3 Bias LSB	*	RO
176		Tx4 Bias MSB	*	RO
177		Tx4 Bias LSB	*	RO
178		Tx5 Bias MSB	*	RO
179		Tx5 Bias LSB	*	RO
180		Tx6 Bias MSB	*	RO
181		Tx6 Bias LSB	*	RO
182		Tx7 Bias MSB	*	RO
183		Tx7 Bias LSB	*	RO
184		Tx8 Bias MSB	*	RO
185		Tx8 Bias LSB	*	RO
186		Rx1 Power MSB	*	RO
187		Rx1 Power LSB	*	RO
188		Rx2 Power MSB	*	RO
189		Rx2 Power LSB	*	RO
190		Rx3 Power MSB	*	RO
191		Rx3 Power LSB	*	RO
192		Rx4 Power MSB	*	RO
193		Rx4 Power LSB	*	RO
194		Rx5 Power MSB	*	RO
195		Rx5 Power LSB	*	RO
196		Rx6 Power MSB	*	RO
197		Rx6 Power LSB	*	RO
198		Rx7 Power MSB	*	RO
199		Rx7 Power LSB	*	RO
200		Rx8 Power MSB	*	RO
201		Rx8 Power LSB	*	RO
202	Configuration Error Codes	Configuration Error Code for lane 1~2	*	RO
203		Configuration Error Code for lane 3~4	*	RO
204		Configuration Error Code for lane 5~6	*	RO
205		Configuration Error Code for lane 7~8	*	RO
206	Active Control Set	Active Set Lane 1 Application code/Data Path code/Explicit Control	10	RO
207		Active Set Lane 2 Application code/Data Path code/Explicit Control	10	RO
208		Active Set Lane 3 Application code/Data Path code/Explicit Control	10	RO
209		Active Set Lane 4 Application code/Data Path code/Explicit Control	10	RO
210		Active Set Lane 5 Application code/Data Path code/Explicit Control	10	RO

211		Active Set Lane 6 Application code/Data Path code/Explicit Control	10	RO
212		Active Set Lane 7 Application code/Data Path code/Explicit Control	10	RO
213		Active Set Lane 8 Application code/Data Path code/Explicit Control	10	RO
214		Active Set Tx1~8 Adaptive Input Eq Enable	FF	RO
215		Active Set Tx1~4 Adaptive Input Eq Recall	*	RO
216		Active Set Tx5~8 Adaptive Input Eq Recall	*	RO
217		Active Set Tx1~2 Input Eq control	*	RO
218		Active Set Tx3~4 Input Eq control	*	RO
219		Active Set Tx5~6 Input Eq control	*	RO
220		Active Set Tx7~8 Input Eq control	*	RO
221		Active Set Tx1~8 CDR control	FF	RO
222		Active Set Rx1~8 CDR control	FF	RO
223		Active Set Rx1~2 Output Eq control, precursor	00	RO
224		Active Set Rx3~4 Output Eq control, precursor	00	RO
225		Active Set Rx5~6 Output Eq control, precursor	00	RO
226		Active Set Rx7~8 Output Eq control, precursor	00	RO
227		Active Set Rx1~2 Output Eq control, postcursor	00	RO
228		Active Set Rx3~4 Output Eq control, postcursor	00	RO
229		Active Set Rx5~6 Output Eq control, postcursor	00	RO
230		Active Set Rx7~8 Output Eq control, postcursor	00	RO
231		Active Set Rx1~2 Output Amplitude control	33	RO
232		Active Set Rx3~4 Output Amplitude control	33	RO
233		Active Set Rx5~6 Output Amplitude control	33	RO
234		Active Set Rx7~8 Output Amplitude control	33	RO

235	reserved		00	RO
236				RO
237				RO
238				RO
239				RO
240	Host Electrical to Module Media Lane Mapping	Module TX media lane 1 wavelength/fiber mapping	11	RO
241		Module TX media lane 2 wavelength/fiber mapping	21	RO
242		Module TX media lane 3 wavelength/fiber mapping	31	RO
243		Module TX media lane 4 wavelength/fiber mapping	41	RO
244		Module TX media lane 5 wavelength/fiber mapping	00	RO
245		Module TX media lane 6 wavelength/fiber mapping	00	RO
246		Module TX media lane 7 wavelength/fiber mapping	00	RO
247		Module TX media lane 8 wavelength/fiber mapping	00	RO
248		Module RX media lane 1 wavelength/fiber mapping	11	RO
249		Module RX media lane 2 wavelength/fiber mapping	21	RO
250		Module RX media lane 3 wavelength/fiber mapping	31	RO
251		Module RX media lane 4 wavelength/fiber mapping	41	RO
252		Module RX media lane 5 wavelength/fiber mapping	00	RO
253		Module RX media lane 6 wavelength/fiber mapping	00	RO
254		Module RX media lane 7 wavelength/fiber mapping	00	RO
255		Module RX media lane 8 wavelength/fiber mapping	00	RO

Digital Diagnostic Monitoring Functions

support the I2C-based Diagnostic Monitoring Interface (DMI) defined in document SFF-8636. The host can access real-time performance of transmitter and receiver optical power, temperature, supply voltage and bias current.

Performance Item	Related Bytes(A0[00] memory)	Monitor Error	Notes
Module temperature	22 to 23	+/-3℃	1，2
Module voltage	26 to 27	< 3%	2
LD Bias current	42 to 43	< 10%	2
Transmitter optical power	50 to 51	< 3dB	2
Receiver optical power	34 to 35	< 3dB	2

Note

1， Actual temperature test point is fixed on module case around Laser.

2， Full operating temperature range

Alarm and Warning Thresholds

support alarms function, indicating the values of the preceding basic perfor-mance are lower or higher than the thresholds.

Performance Item	Alarm Threshold Bytes(A0[02] memory)	Unit	Low thresh-old	High thresh-old
Temp Alarm	128 to 131	℃	-10	80
Temp Warning	132 to 135	℃	0	70
Voltage Alarm	144 to 147	V	2.97	3.63
Voltage Warn-ing	148 to 151	V	3.135	3.465
TX Power Alarm	176 to 179	dBm	-6.3	6.5
TX Power Warning	180 to 183	dBm	-3.3	3.5
RX Power Alarm	192 to 195	dBm	-10.6	6.5
RX Power Warning	196 to 199	dBm	-7.6	3.5

Mechanical Specifications

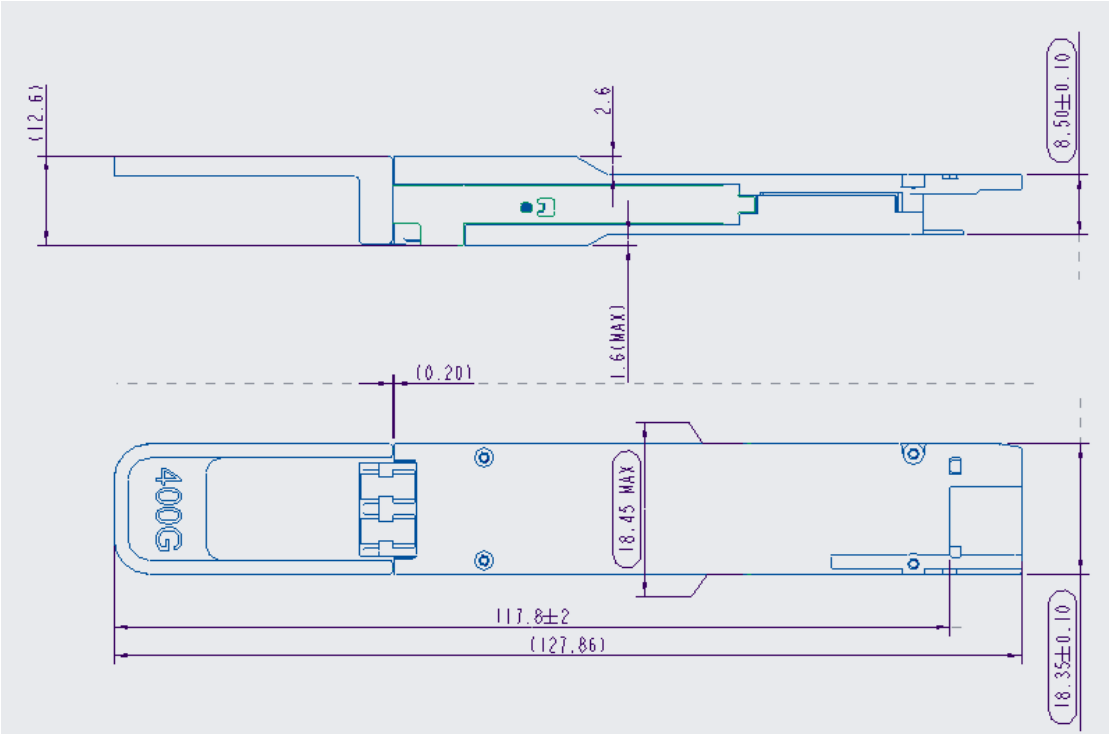

Figure 5. Mechanical Dimensions

Regulatory Compliance

Optical Transceiver is RoHS 6/6 compliant and complies with international electromagnetic compatibility (EMC) and product safety requirements and standards.

Feature	Agency	Standard	Performance
Safety	NRTL	UL 62368-1 CAN/CSA C22.2 No. 62368-1	NRTL recognized component for US and CAN
	TUV	EN 62368-1 IEC 60825-1:2014 EN 60825-1:2014 IEC 60825-2:2004+A1:2006+A2:2010 EN 60825-2:2004+A1:2006+A2:2010	TUV certificate

	FDA	U.S. 21 CFR 1040.10	FDA/CDRH certified with accession number according to Laser Notice 56
Electromagnetic Compatibility	Radiated emissions	EMC Directive 2014/30/EU EN 55032 CISPR 32 FCC rules 47 CFR Part 15 ICES-003 AS/NZS CISPR 32	Class B digital device with a minimum -6dB margin to the limit when tested with a metal enclosure. Final margin may vary depending on system application, good system EMI design practice, ie: suitable metal enclosure and well-bonding, is required to achieve Class B margins at the system level. Tested frequency range: 30 MHz to 40 GHz or 5th harmonic (5 times the highest frequency), whichever is less.
	ESD	EMC Directive 2014/30/EU EN 55035 CISPR 35 IEC/EN 61000-4-2	Withstands discharges of ±8 k V contact, ±15 k V air.
	Radiated immunity	EMC Directive 2014/30/EU EN 55035 CISPR 35 IEC/EN 61000-4-3	Field strength of 10 V/m from 80 MHz to 6 GHz.
Restriction of Hazardous Substances	RoHS	EU Directive 2011/65/EU （EU）2015/863	

ESD Design

Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and otherwise handled in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Parameter	Threshold value	Notes
ESD of high-speed pins	1KV	Human Body Model
ESD of low-speed pins	2KV	Human Body Model
Air discharge during operation	15KV	
Direct contact discharges to the case	8KV	

Safety Specification Design

Cautions

Do not look into fiber end faces without eye protection using an optical meter (such as magnifier and microscope) within 100 mm, unless you ensure that the laser output is disabled.

When operating an optical meter, observe the operation requirements.

CAUTION: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.